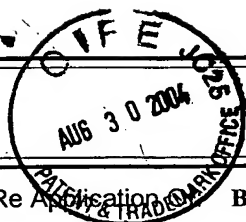


IFW



**TRANSMITTAL LETTER**  
(General - Patent Pending)

Docket No.  
FIS920030190 (00750482AA)

In Re Application of Belyansky et al.

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/695,752	10/30/2003	E. Wojciechowicz	30743	2815	6187

Title: **STRUCTURE AND METHOD TO IMPROVE CHANNEL MOBILITY BY GATE ELECTRODE STRESS MODIFICATION**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

**Response to Requirement for Restriction  
Postcard**

in the above identified application.

- ☒ No additional fee is required.
  - ☐ A check in the amount of \_\_\_\_\_ is attached.
  - ☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0458** as described below.
    - ☐ Charge the amount of \_\_\_\_\_
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Signature

Dated: August 30, 2004

Marshall M. Curtis  
Reg. No. 33,138

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(703) 787-9400

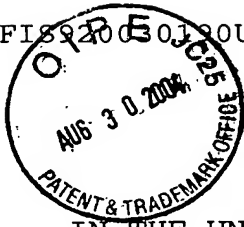
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] o.

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CC:



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of  
 Michael P. Belyansky et al. Conf. No.: 6187  
 Serial No.: 10/695,752 Group Art Unit: 2815  
 Filed: October 30, 2003 Examiner: E. Wojciechowicz  
 For: STRUCTURE AND METHOD TO IMPROVE CHANNEL MOBILITY  
 BY GATE ELECTRODE STRESS MODIFICATION

Commissioner for Patents  
 United States Patent and Trademark Office  
 P. O. Box 1450  
 Alexandria, Virginia 22313-1450

RESPONSE TO REQUIREMENT FOR RESTRICTION

Sir:

In response to the Office Action mailed July 28, 2004, Applicants provisionally elect, without traverse, the invention as defined by the claims of Group II, claims 1 - 12, as identified by the Examiner, for further prosecution on their merits.

REMARKS

Claims 1 - 20 remain active in this application. No new matter has been introduced into the application.

Restriction has been required between the inventions, as identified by the Examiner, of Group I, claims 13 - 20, directed to a semiconductor device, and Group II, claims 1 - 12, directed to a method of making a semiconductor device. Provisional election of the invention of Group II, claims 1 - 12, has been made without traverse, above.